In the Claims

CLAIMS

Claims 1-48 (Canceled).

49. (Previously presented) A semiconductive processing method, comprising:

forming a masking layer over a semiconductive substrate;

forming an opening through the masking layer and partially into the semiconductive substrate, the masking layer comprising a sidewall formed along a periphery of the opening; and

etching a portion of the sidewall to leave a first segment of the sidewall substantially unchanged and to form a second segment of the sidewall laterally spaced from and elevationally above the first segment, the second segment being substantially parallel with the first segment.

50. (Previously presented) The method of claim 49 further comprising oxidizing the semiconductive substrate to form an oxide beneath the first segment, the oxide lifting the first segment away from the semiconductive substrate.

51. (Previously presented) The method of claim 49 further comprising oxidizing the semiconductive substrate to form an oxide within the opening and beneath the first segment, the oxide lifting the first segment away from the semiconductive substrate and partially filling the opening.

52. (Previously presented) The method of claim 49 wherein the etching of the portion of the sidewall comprises utilizing phosphoric acid.

53. (Previously presented) The method of claim 49 further comprising extending the opening into the semiconductive substrate after the etching of the portion of the sidewall.

54. (Previously presented) The method of claim 49 further comprising filling the opening with insulative material.

55. (Previously presented) The method of claim 49 wherein the masking layer comprises silicon nitride.

56. (Previously presented) A semiconductive processing method, comprising:

forming a masking layer over a semiconductive substrate;

forming an opening through the masking layer and partially into the semiconductive substrate, the masking layer comprising a sidewall formed along a periphery of the opening; and

etching a portion of the sidewall, the etching comprising:

forming a first segment of the sidewall substantially unchanged;

forming a second segment of the sidewall laterally spaced from and elevationally above the first segment; and

forming a third segment being formed between and connecting the first and second segments at respective right angles.

57. (Previously presented) The method of claim 56 wherein the third segment comprises an exposed upper surface of the masking layer.

58. (Currently amended) The method of claim 56 wherein the etching of the portion of the sidewall further comprises performing a ~~dry~~ wet etch procedure.

59. (Previously presented) The method of claim 56 wherein the third segment comprises an exposed upper surface elevationally below an uppermost surface of the of the masking layer, and further comprising forming another masking layer over the uppermost surface.

60. (Previously presented) The method of claim 56 further comprising oxidizing the semiconductive substrate to form an oxide beneath the first segment, the oxide lifting the first segment away from the semiconductive substrate.

61. (Previously presented) The method of claim 56 wherein the masking layer comprises silicon nitride.

62. (Previously presented) The method of claim 56 further comprising filling the opening in the semiconductive substrate with insulative material.

63. (Previously presented) A semiconductive processing method, comprising:

forming a first masking layer over a semiconductive substrate;

forming a second masking layer over the first masking layer;

forming an opening through the first and second masking layers and partially into the semiconductive substrate, the first and second masking layers comprising respective sidewalls formed along a periphery of the opening;

etching the sidewall of the second masking layer laterally from the opening and exposing an upper surface portion of the first masking layer, the etching forming a second sidewall of the second masking layer; and

etching the upper surface portion of the first masking layer to leave a first segment of the sidewall of the first masking layer substantially unchanged and to form a second segment of the sidewall of the first masking layer which is aligned with the second sidewall of the second masking layer.

64. (Previously presented) The method of claim 63 wherein the first masking layer comprises silicon nitride and the second masking layer comprises photoresist.

65. (Previously presented) The method of claim 63 wherein the semiconductive substrate comprises a sidewall formed along the periphery of the opening, and wherein the first segment of the sidewall of the first masking layer is formed in alignment with the sidewall of the semiconductive substrate.

66. (Previously presented) The method of claim 63 wherein the etching of the sidewall of the second masking layer comprises performing a dry etch procedure.

67. (Previously presented) The method of claim 63 wherein the etching of the sidewall of the second masking layer comprises performing a dry etch procedure utilizing an oxygen-containing material.

68. (Previously presented) The method of claim 63 wherein the etching of the sidewall of the second masking layer comprises performing a dry etch procedure utilizing a mixture of O_2 and He.

69. (Previously presented) The method of claim 63 wherein the etching of the upper surface portion of the first masking layer comprises utilizing phosphoric acid.